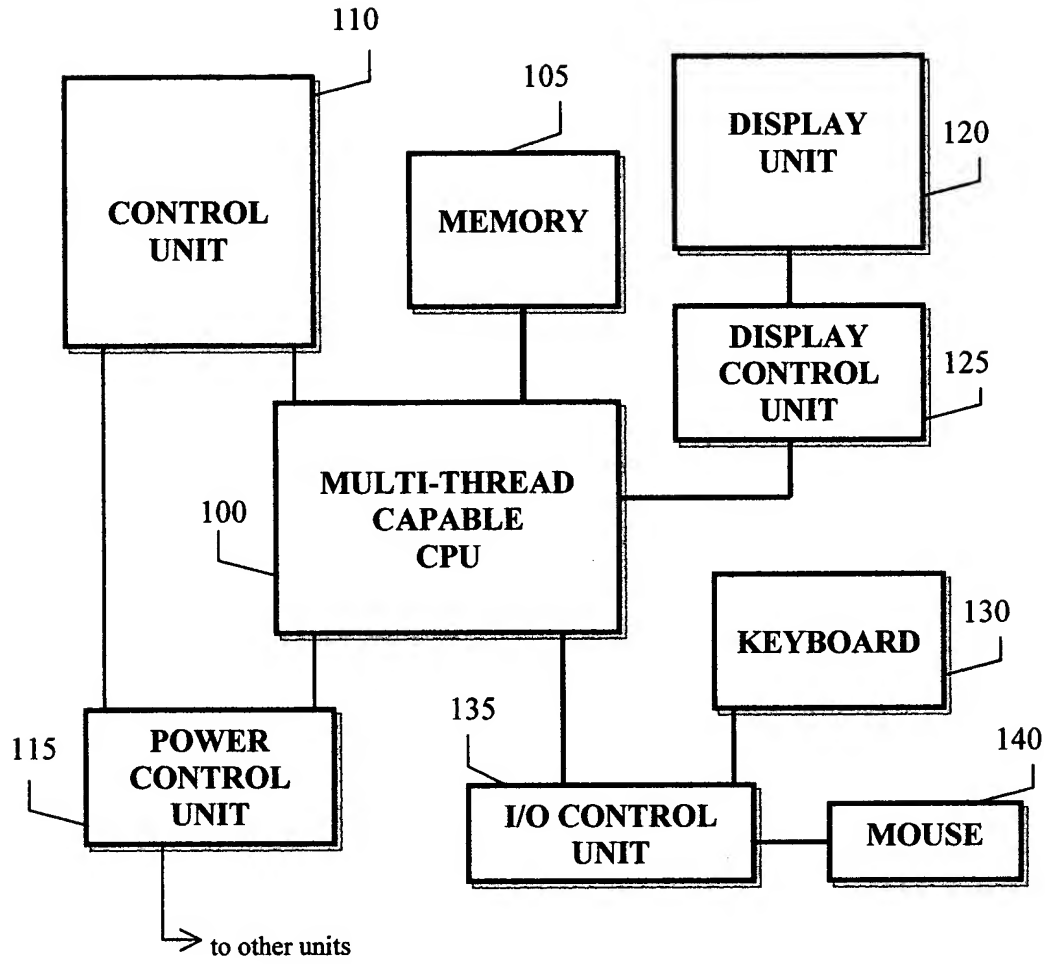
110
CONTROL UNIT
105
MEMORY
DISPLAY UNIT
120
DISPLAY CONTROL UNIT
125
MULTI-THREAD CAPABLE CPU
100
KEYBOARD
130
135
140
115
POWER CONTROL UNIT
I/O CONTROL UNIT
MOUSE
to other units

Figure 1

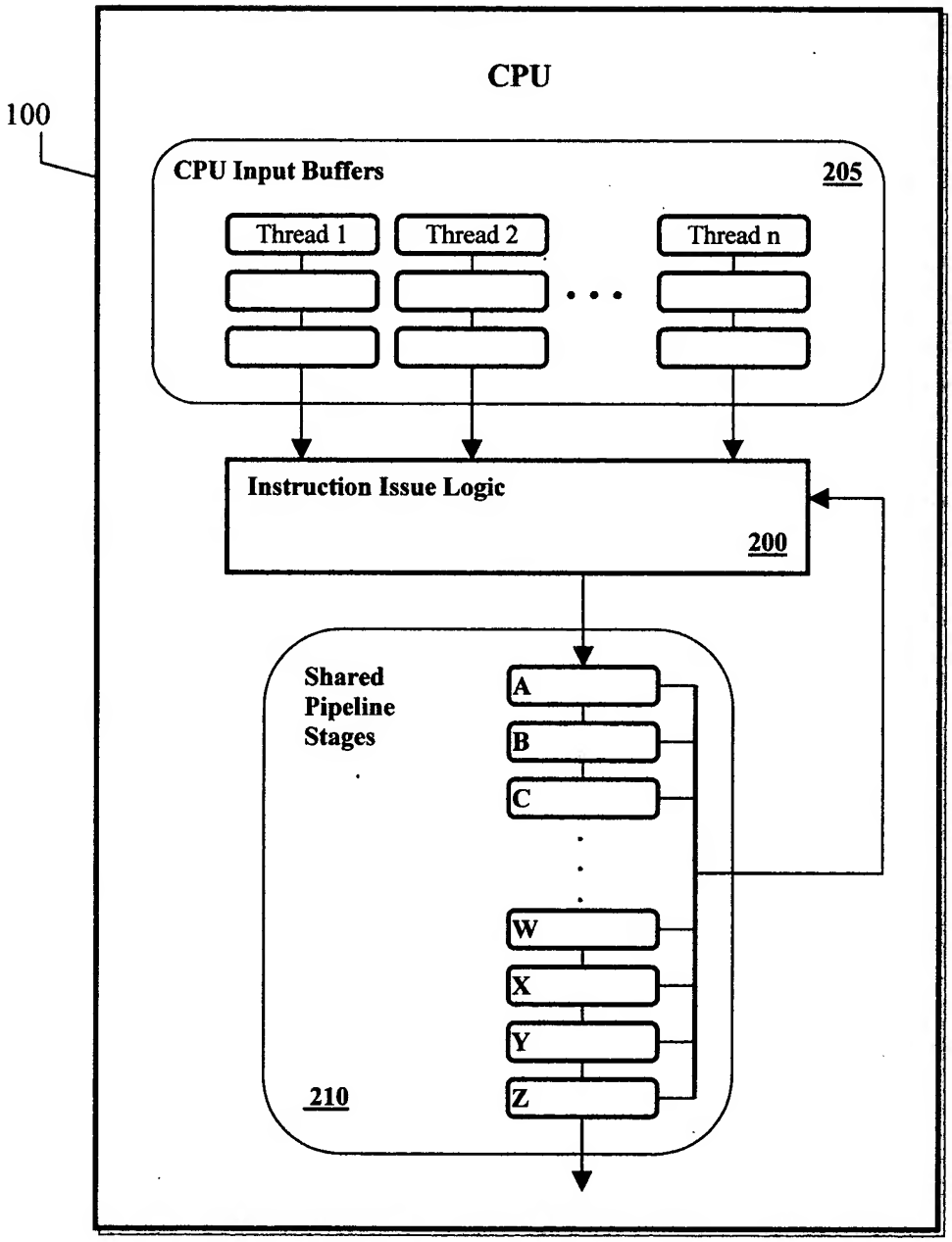
CPU
100
CPU Input Buffers
205
Thread 1
Thread 2
Thread n
Instruction Issue Logic
200
Shared
Pipeline
Stages
A
B
C
W
X
Y
Z
210

Figure 2

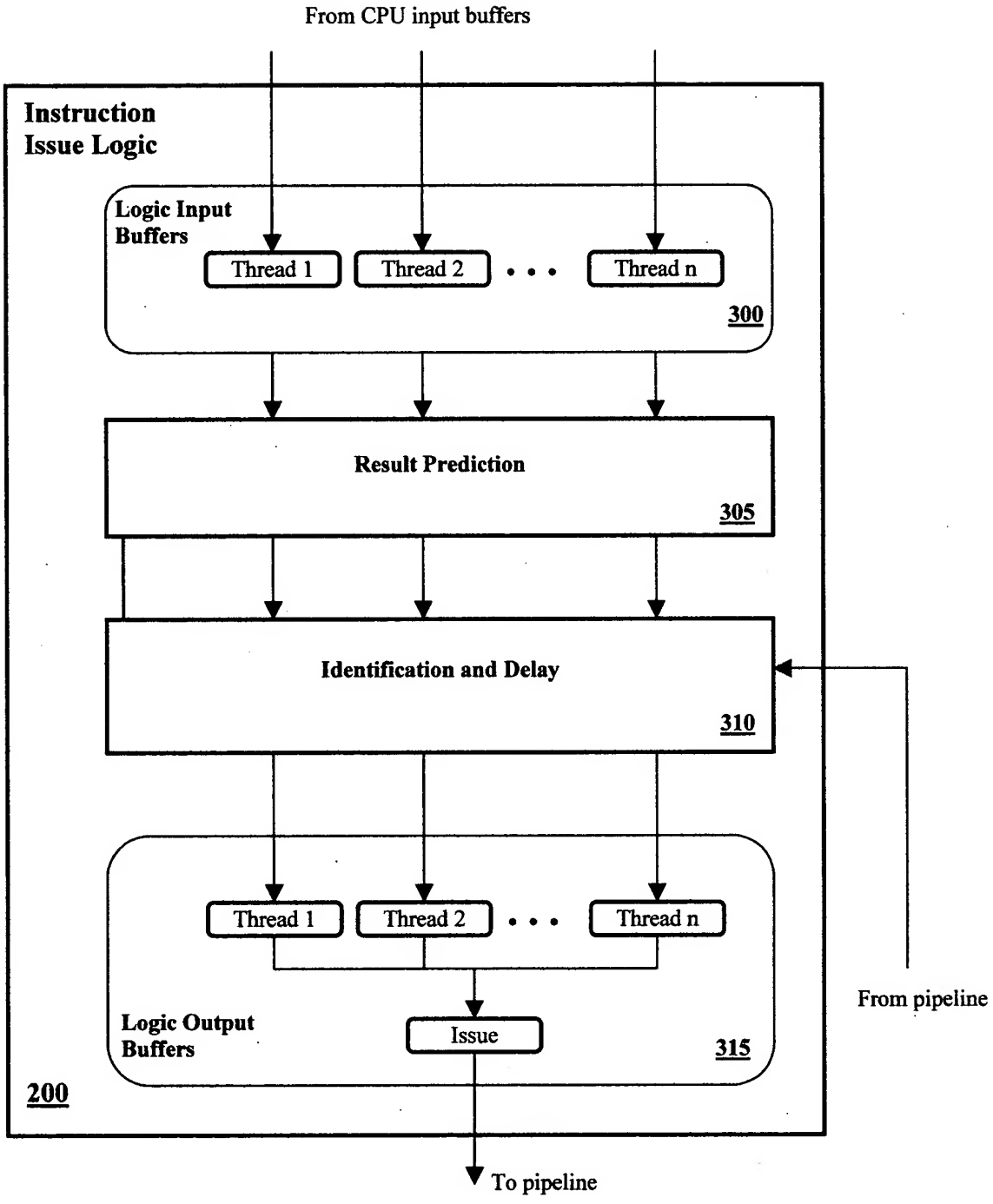
From CPU input buffers
Instruction Issue Logic
Logic Input Buffers
Thread 1
Thread 2
Thread n
300
Result Prediction
305
Identification and Delay
310
Thread 1
Thread 2
Thread n
Logic Output Buffers
Issue
315
200
From pipeline
To pipeline

Figure 3

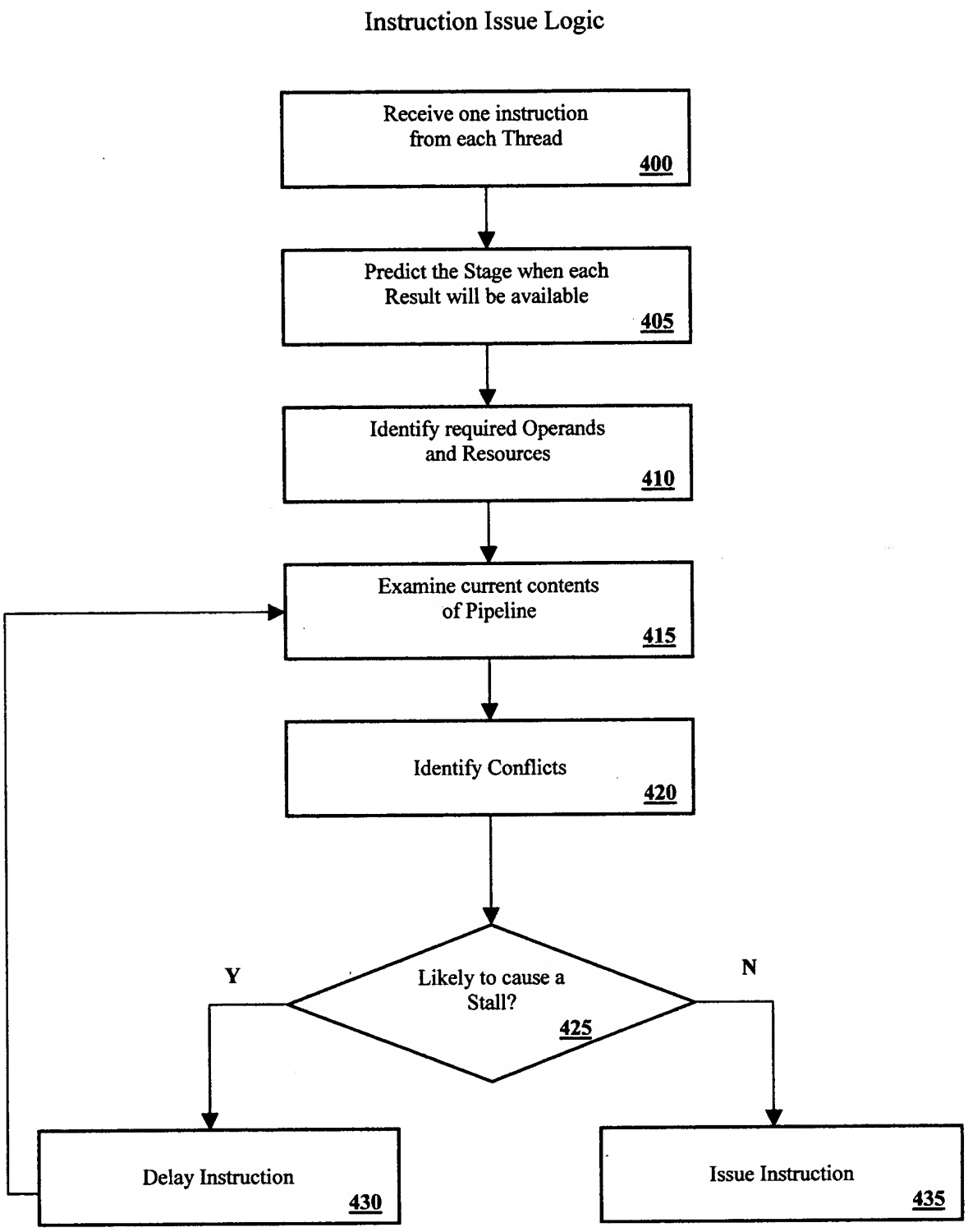
Instruction Issue Logic
Receive one instruction from each Thread
400
Predict the Stage when each Result will be available
405
Identify required Operands and Resources
410
Examine current contents of Pipeline
415
Identify Conflicts
420
Likely to cause a Stall?
425
Y
N
Delay Instruction
430
Issue Instruction
435

Figure 4

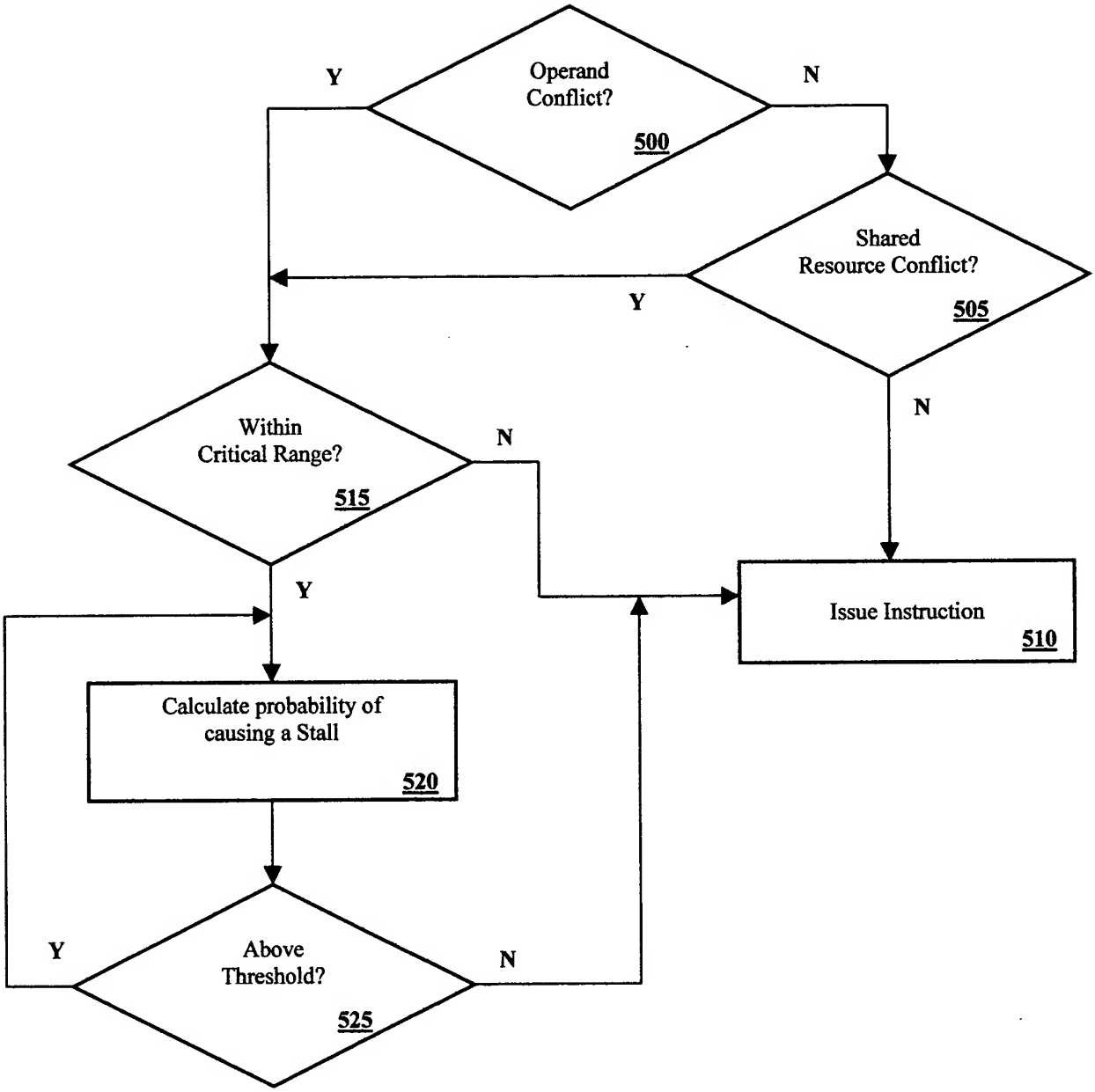
Operand Conflict?
500
Y
N
Shared Resource Conflict?
505
Y
N
Within Critical Range?
515
N
Y
Issue Instruction
510
Calculate probability of causing a Stall
520
Above Threshold?
525
Y
N

Figure 5

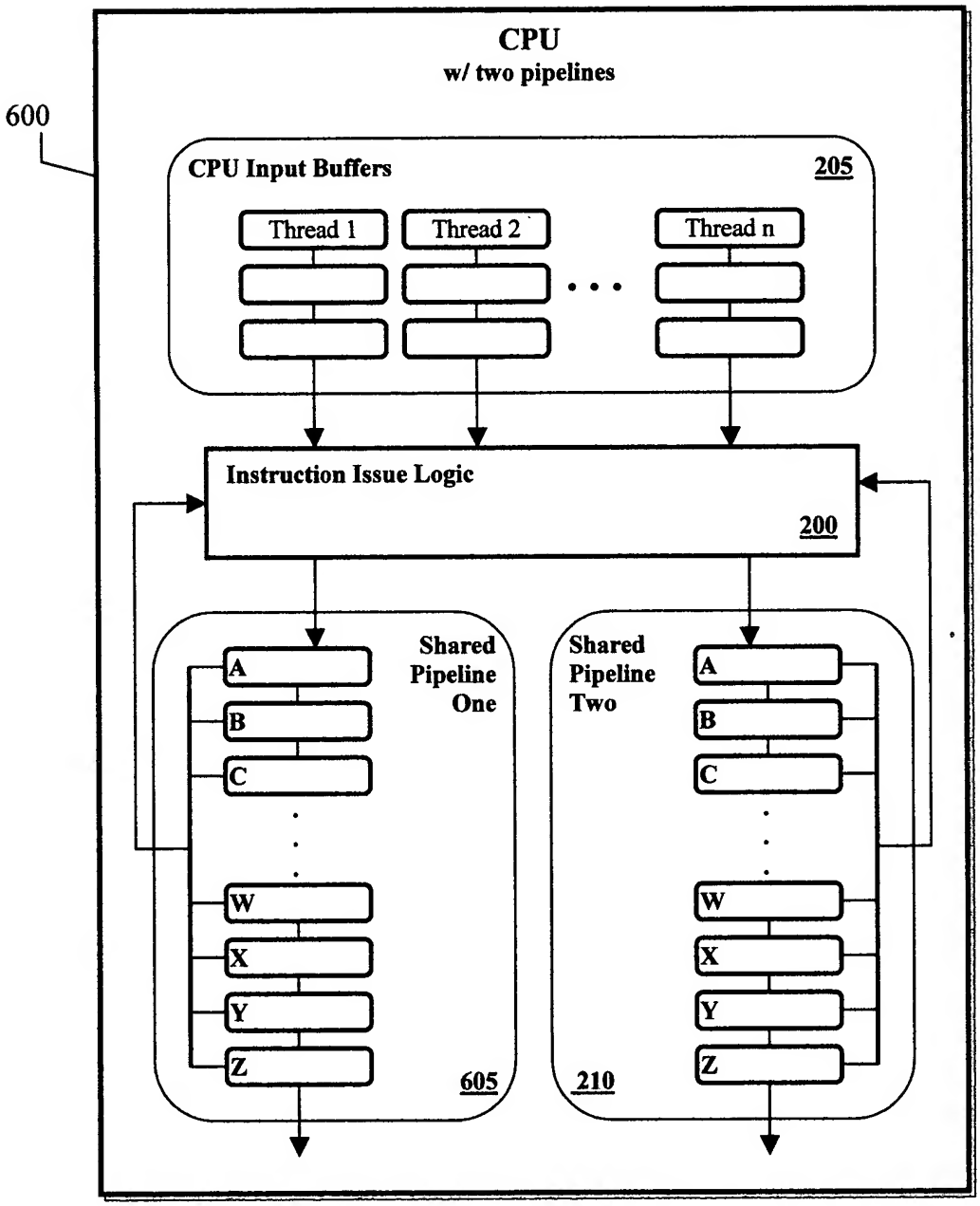
CPU
w/ two pipelines
600
CPU Input Buffers
205
Thread 1
Thread 2
Thread n
Instruction Issue Logic
200
Shared Pipeline One
Shared Pipeline Two
A
B
C
W
X
Y
Z
605
210

Figure 6